

## GEORGE K CELLER

Research Professor, Institute for Advanced Materials, Devices, and Nanotechnology  
Materials Science and Engineering Department, Rutgers University  
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### EDUCATION

Ph.D. in Physics, Purdue University (1976). Thesis on "Modulation of acoustoelectric interactions and optical properties of GaAs by intense laser light".

M.Sc. in Physics, University of Warsaw, Poland (1969).

### WORK EXPERIENCE

#### **Research Professor, IAMDN and MSE, Rutgers University, Piscataway, NJ, 2010 –**

Investigating heterogeneous integration of thin device-quality SiC layers, produced by ion-cutting, with silicon and other substrates. Developing concepts for laser assisted ion-cutting.

#### **Consultant to Soitec and other companies, 2010-2012**

Topics: Silicon photonics, SOI, wafer bonding, semiconductor processing, SEMI Standards, and ITRS.

#### **Soitec, Peabody, MA, and Grenoble, France, 2001–2009.**

*Chief Scientist.* Responsible for technical programs in the US and for joint development activities with Soitec's partners, such as IBM, in the areas of SOI (silicon-on-insulator), strained SOI, Smart Cut technology, and layer transfer applications. Member of a Photovoltaic Taskforce. Arranging and leading interactions with academia, e.g., Univ. of Wisconsin, MIT, Stanford, Univ. of Florida, Purdue, SUNY (Albany), Johannes Kepler Univ. (Linz, Austria).

#### **Bell Laboratories, Murray Hill, New Jersey, 1979–2001.**

*Technical Manager and Distinguished MTS in Silicon Processing Research Department, 1996-2001.* Characterization of silicon-on-insulator substrates and fabrication of advanced devices and circuits in SOI.

*Technical Manager in Advanced Lithography Research, 1990–1996.* Technical, financial, and administrative management of a proximity x-ray lithography group of about 20 people. Interacted closely with DARPA and NRL program sponsors. During 1993 –1996 was also a Deputy Program Manager for the National X-Ray Lithography Association, which included teams from AT&T, IBM, Motorola and Loral.

*Supervisor in Electronic Materials Research Department 1984–1990.* Initiated the first amorphous silicon active matrix display program in AT&T and building of optically reconfigurable artificial neural networks. Led a program at Murray Hill, Allentown, and Reading, PA, to improve the microstructure and manufacturing methods for dielectrically isolated gated diode switches. Studied diffusion and thermomigration phenomena in silicon dioxide and formation of spherical nanoclusters of Ge, As, Sb, and P in SiO<sub>2</sub>.

*Member of Technical Staff in Electronics Materials Research Department 1979 –1984.* Pioneered the development of Rapid Thermal Processing (RTP), built the largest and most versatile RTP system at the time, and invented unique applications of this technique. Revolutionized SIMOX (SOI made by O<sup>+</sup> implantation and annealing) formation by using inherently stable annealing at 1405 C, 7 degrees below the Si melting point. Developed methods of controlled laser melting and subsequent recrystallization of thin silicon films.

#### **Western Electric Engineering Research Center in Princeton, NJ, 1976 –1979.**

*Member of Research Staff in Laser Studies Group.* Investigated interactions of intense light beams with materials, laser annealing of ion-implanted semiconductors.

**International Atomic Energy Agency (IAEA), Vienna, Austria, 1970 (June–Dec).**

Researcher in the Hydrology Section, studied tritium distribution in water over large geographic areas.

**University of Vienna, Austria, Dec. 1969–May 1970.**

Research Associate, investigated hot carrier transport in silicon

**RESEARCH INTERESTS**

Heterogeneous integration of single crystalline SiC with other electronic substrates  
Electronic materials – processing and characterization  
Silicon-on-Insulator (SOI) formation and applications (electronic, photonic, MEMS)  
Thin films, strained layers, layer transfer  
Laser processing of materials  
Integrated photonics and optical communications  
Photovoltaic materials and devices

**HONORS AND AWARDS**

Outstanding Mentor Award of SiWEDS (Si Wafers Eng. and Defects Science) Research Consortium (2008).

SEMI Merit Award (2007).

Bell Labs President's Gold Award for Lambda Router (optical MEMS) (2000).

Bell Labs President's Gold Award for the 0.25  $\mu\text{m}$  Si technology (1999).

Fellow of the Electrochemical Society (1994).

Electronics Division Award of the Electrochemical Society (1993).

Distinguished Member of Technical Staff Award at AT&T Bell Labs (1992).

Fellow of the American Physical Society (1990).

**EXTERNAL FUNDING (while at Bell Labs)**

I was instrumental in obtaining a \$10.5 million, 42-month contract from DARPA to support the Bell Labs x-ray lithography program that I led.

**PROFESSIONAL COMMITTEES**

**Associate Editor** – ECS Journal of Solid State Science and Technology, and ECS Solid State Letters, since 2011.

**ITRS** - Chair of the SOI sub-TWG of Starting Materials 2001–2012, member since 1996.

**SEMI Standards** - Chair of the SOI Task Force 2002–2012. Member of North American Regional Silicon Standards Committee since 2000. Received several Appreciation Awards.

**SiWEDS** - Vice-Chair of Industrial Advisory Board 2007–2009.

**MIT Microphotonics Consortium** - Member of the Board since 2005.

**PROFESSIONAL SOCIETIES AND ACADEMIC ACTIVITIES**

**The Electrochemical Society**

Chair of the Electronics Division (1993 – 95) and 2<sup>nd</sup> vice-chair 1991–1993.

Member of the Board of Directors of the Society (1993–1995)

Member of the Executive Committee of the Electronics and Photonics Division since 1985.

Chair of the Electronics and Photonics Division Award Committee (1998–2003, and 2009–2010).

On the Advisory Board of the ECS Interface (1999-2010).

**IEEE**

**International Silicon-on-Insulator Conference:** Local Arrangements Chair (1984), Technical Chair (1985) and General Chair (1986). Member of the Program Committee, 1987–1990, and again from 2000 to 2003.

**MRS:** One of three "Volume Organizers" for the 2002 issues of the MRS Bulletin.

**Fellow of APS, member of OSA.**

**Georgia Inst. of Technology:** Member of the External Advisory Board of NSF funded Materials Research and Engineering Center (MRSEC) on Epitaxial Graphene, since 2009.

**LAAS Institute, Toulouse, France:** Member of a Ph.D. committee for two students who graduated in 2001, and 2006.

**NJIT:** External evaluator at the NJ Institute of Technology for a proposed M.Sc./Ph.D. Program in Materials Science and Engineering, (1996).

**Univ. of Wisconsin:** Industrial mentor for the SRC x-ray mask program, (1992–1994)

**NCSU:** taught a short course on SOI, 1989.

#### **EXTERNAL ACTIVITIES AT SOITEC**

- Technical Chair, 2002 SOI Technical Workshop, Sainte-Maxime, France (27 invited speakers from three continents).
- Technical Chair, 2006 SOI Forum, Megeve, France (28 invited industry leaders from Japan, Singapore, Europe and the US).
- Coordinator of a Joint Development Program at IBM, Yorktown Heights, 2007–2008.
- Member of a Photovoltaic Taskforce, whose recommendations led to an acquisition by Soitec of a German PV company, Concentrix Solar, 2008 – 2009.
- Lecturer at MIGAS'2004, Summer School on "Silicon on Insulator: Technology and Devices" (Villard de Lans, France, June 26 – July 2, 2004).

#### **BELL LABORATORIES AND WESTERN ELECTRIC**

- Program manager for DARPA funded X-Ray lithography program at Bell Labs, 1992–1996.
- Deputy Program Manager for the National X-ray Lithography Association. Represented AT&T and worked with managers from IBM, Motorola, and Loral, 1993–1996.
- Organized the first Bell System Laser Annealing Symposium in 1977 (which was likely the first significant laser annealing technical conference anywhere outside the Soviet Union).
- Recruiter at Purdue for SRP (Summer Research program), CRFP, and GRPW (Graduate Research Program for Women).
- Mentor for SRP and GRPW students at Bell Labs.
- Mentor for postdocs: Helmut Baumgart, Ratnaji Kola, and Hershel Marchman,
- Mentor for Lee Trimble's M.Sc. program in Materials Science at Stevens (completed in 1986).
- Representative to Library Users' Committee (1989–1994).
- Represented Lucent on the SRC TAB for Materials and Bulk Processes (MBPS), later renamed Front End Processes, attended reviews, reviewed proposals, coordinated Lucent team responses to SRC. (1996 – 2001)
- Represented Lucent at the SRC FEP Center for high k dielectrics, with its main location at the NCSU. (1999 – 2001).
- Member of SOI PTAB at SEMATECH, 1996–1998
- Member of the SEMATECH X-Ray Lithography Working Group, 1992–1994.
- Member of the NIST/DARPA X-Ray Mask Standards Committee, 1992–1995.

## CONFERENCE ORGANIZER AND PROCEEDINGS EDITOR

1. **Silicon-on-Insulator Technology and Devices 13**, Editor: G. K. Celler; Assistant Editors: S. Cristoloveanu, S. W. Bedel, F. Gamiz, B.-Y. Nguyen, and Y. Omura, ECS Transactions Vol. 6, No. 4, 395 pages (The Electrochemical Society, Pennington, NJ, 2007).
2. **Silicon-on-Insulator Technology and Devices XII**, Editor: G. K. Celler; Assistant Editors: S. Cristoloveanu, J. G. Fossum, F. Gamiz, and K. Izumi, ECS Proc. Vol. PV 2005-03, 396 pages (The Electrochemical Society, Pennington, NJ, 2005).
3. **Silicon-on-Insulator Technology and Devices XI**, Editor: S. Cristoloveanu; Assistant Editors, G. Celler J. Fossum, F. Gamiz, K. Izumi, and Y.-W. Kim, ECS Proc. Vol. PV 2003-05, 522 pages (The Electrochemical Society, Pennington, NJ, 2003).
4. **Silicon-on-Insulator Technology and Devices X**, Editors: S. Cristoloveanu, P. L. F. Hemment, K. Izumi, G. K. Celler, F. Assaderaghi, and Y.-W. Kim, ECS Proc. Vol. PV 2001-03, 463 pages (The Electrochemical Society, Pennington, NJ, 2001).
5. **ULSI Science and Technology 1993**, edited by George K. Celler, Ed Middlesworth, and Koichiro Hoh, ECS Proc. Vol. PV 1993-13, 306 pages (The Electrochemical Society, Pennington, NJ, 1993).
6. **Materials Aspects of X-Ray Lithography**, edited by George K. Celler and Juan R. Maldonado, MRS Symp. Proc. Vol. 306, 291 pages (Materials Research Society, Pittsburgh, PA, 1993).
7. **ULSI Science and Technology 1991**, edited by John M. Andrews and George K. Celler, ECS Proc. Vol. 91-11, 924 pages (The Electrochemical Society, Pennington, NJ, 1991).
8. **Laser and Electron-Beam Interactions with Solids**, edited by B. R. Appleton and G. K. Celler, MRS Symp. Proc. Vol. 4, 812 pages (Elsevier Science Publishing Co, New York, 1982).
9. **Laser and Electron Beam Processing of Electronic Materials**, edited by C. Lawrence Anderson, George K. Celler, and George A. Rozgonyi, ECS Proc. Vol. 80-1, 550 pages (The Electrochemical Society, Princeton NJ, 1980)

## CONFERENCE ORGANIZER WITHOUT PROCEEDINGS

1. Symposium on Electronic and Photonic materials for the 21<sup>st</sup> Century (ECS), organized by G. K. Celler, Toronto, May 2000.
2. Rapid Thermal Processing of Electronic Materials Symposium (ECS), organized by G. K. Celler and S. J. Pearton, 1988.

## OTHER CONFERENCE COMMITTEES

1. International Conference on Semiconductor Technology for Ultra Large Scale Integrated Circuits and Thin Film Transistors (ULSIC vs. TFT), Xian, China, July 5–10, 2009.
2. The International Conference on Electron, Ion, and Photon Beam Technology (EIPB) (1991–1997).
3. Soc. Photo-Optical Instrumentation Engineers (SPIE) Lithography Symposia, (1990–1997).
4. ULSI Symposium of the ECS (1983–1997).
5. IEEE SOI Conference (1984–1990 and 2002–2005).
6. MRS Beam-Solid Interactions Symposium (1979–1987).

7. Conference on Lasers and Electro-Optics (CLEO) (1978–1980).

## PATENTS

**(Recently filed, assigned to Rutgers):** G. K. Celler, THIN EPITAXIAL SILICON CARBIDE WAFER FABRICATION, filed 1-24-2014, (Rutgers No. 2014-002).

1. G. K. Celler, Substrates for Monolithical Optical Circuits and Electronic Circuits, U.S. Patent 8,299,485 B2, issued Oct. 30, 2012.
2. O. Kononchuk and G. K. Celler, Oxidation after Oxide Dissolution, U.S. Patent 8,148,242, issued April 3, 2012.
3. G. K. Celler, Relaxation of a Strained Layer Using a Molten Layer, U.S. Patent 7,968,911, issued June 20, 2011.
4. G. K. Celler, Method of Forming a Device Wafer with Recyclable Support, U.S. Patent 7,956,436, issued June 7, 2011.
5. G. K. Celler, Wafer with Diamond Layer, U.S. Patent 7,605,055, issued Oct. 20, 2009.
6. G. K. Celler, Method of Forming a Device Wafer with Recyclable Support, U.S. Patent 7,605,054, issued Oct. 20, 2009.
7. G. K. Celler, Relaxation of a Strained Layer Using a Molten Layer, U.S. Patent 7,585,792, issued Sept. 8, 2009.
8. G. K. Celler and Y. J. Chabal, Single Crystal Silicon on Polycrystalline Silicon Integrated Circuits, U.S. Patent 6,388,290, issued May 14, 2002.
9. J. A. Abate, G. K. Celler, and J. V-Y. Guo, Process for Making an X-ray Mask. U. S. Patent 5,656,399, issued Aug. 12, 1997.
10. G. K. Celler, L. R. Harriott, and R. R. Kola, Material Removal with Focused Particle Beams U. S. Patent 5,482,802, issued Jan. 9, 1996.
11. G. K. Celler and L. E. Trimble, X-ray Lithography Mask and Devices Made Therewith. U. S. Patent 5,051,326, issued Sept. 24, 1991.
12. G. K. Celler and L. E. Trimble, As Drift in Silicon Dioxide and Formation of Buried Conductive Layers. U. S. Patent 4,835,113, issued May 30, 1989.
13. G. K. Celler, Fabrication of Dielectrically Isolated Devices Utilizing Buried Oxygen Implant and Subsequent Heat Treatment at Temperatures above 1300C. U. S. patent 4,676,841 issued June 30, 1987.
14. G. K. Celler, D. G. Schimmel, P. K. Roy, and L. E. Trimble, Process for Fabricating Dielectrically Isolated Devices Utilizing Heating of Polycrystalline Support Layer to Prevent Substrate Deformation. U. S. patent 4,581,814 issued April 15, 1986.
15. G. K. Celler and McD. Robinson, Dielectrically Isolated Silicon Devices. U. S. patent 4,497,683 issued Feb. 5, 1985.

16. G. K. Celler, D. J. Lischner and McD. Robinson, Dielectrically Isolated Silicon Devices. U. S. patent 4,494,303 issued Jan. 22, 1985.
17. G. K. Celler, D. J. Lischner, and McD. Robinson, Process for Producing Silicon Devices. U. S. patent 4,461,670 issued Jul. 24, 1984.
18. G. K. Celler, H. J. Leamy, and L. E. Trimble, Method of Increasing the Grain Size of Polycrystalline Materials by Directed Energy-Beams, U. S. patent 4,406,709 issued Sept. 27, 1983.
19. G. K. Celler and T. E. Seidel, Metallization for Integrated Circuits. U. S. Patent No. 4,258,078 issued Mar. 24, 1981.
20. G. K. Celler, Method of Removing Contaminating Impurities from Device Areas in a Semiconductor Wafer. U.S. patent 4,249,962 issued Feb 10, 1981.
21. G. K. Celler and G. L. Miller, Forming Self-Guarded p-n Junctions by Epitaxial Regrowth of Amorphous Regions Using Selective Radiation Annealing. U. S. Patent No. 4,240,843 issued Dec. 23, 1980.
22. G. K. Celler, L. C. Kimerling, H. J. Leamy, J. M. Poate, G. A. Rozgonyi, Patterned Epitaxial Regrowth Using Overlapping Pulsed Irradiation. U. S. Patent No. 4,234,358 issued Nov.18, 1980.

#### CHAPTERS IN EDITED VOLUMES AND REVIEW ARTICLES

1. **SOI Materials and Devices**, S. Cristoloveanu and G. K. Celler, Chapter 4 of *Handbook of Semiconductor Manufacturing Technology, 2<sup>nd</sup> edition*, edited by R. Doering and Y. Nishi (CRC Press, Taylor and Francis Group, Boca Raton, FL, 2007), pp. 4-1 through 4-52. (DOI: 10.1201/9781420017663.ch4)
2. **Advanced High-Mobility Semiconductor-On-Insulator Materials**, B. Ghyselen, I. Cayrefourcq, M. Kennard, F. Letertre, T. Akatsu, G. Celler, and C. Mazuré, Chapter 3 in "*Advanced Gate Stacks for High Mobility Semiconductors* edited by A. Dimoulas, E. Gusev, P. McIntyre and M. Heyns (Springer Series in Advanced Microelectronics, Vol. 27, pp. 43-72, 2007).
3. **Advanced Electronic Substrates for the Nanotechnology Era**, Carlos Mazuré and George K. Celler, *The Electrochemical Society Interface*, Vol. 15, No. 4, pp. 33-40 (January 2007).
4. **Silicon on Insulator by the Smart Cut™ process**, G. K. Celler, A. J. Auberton-Hervé, B. Aspar, C. Lagahe-Blanchard, and C. Maleville, in *Wafer Bonding, Applications and Technology*, edited by M. Alexe and U. Gösele, (Springer, Berlin, New York), pp. 85-106 (2004).
5. **Frontiers of silicon-on-insulator**, G. K. Celler and Sorin Cristoloveanu, *J. Appl. Phys.* **93**, pp. 4955-4978 (2003).
6. **Silicon-on-Insulator Structures: Fabrication**, G. K. Celler, *The Encyclopedia of Advanced Materials*, Pergamon Press 1994.
7. **Buried Oxide and Silicide Formation by High-Dose Implantation in Silicon**, Materials Research Society Bulletin, G. K. Celler and Alice E. White, **17**, (6), 40 (June 1992).
8. **Silicon on Insulators**, G. K. Celler, *The Concise Encyclopedia of Electronic and Optoelectronic Materials*, (Pergamon Press 1992).

9. **Laser - Solid Interactions**, G. K. Celler, *Encyclopedia of Science and Technology*, 6th edition (McGraw Hill, New York 1987), Vol. 9, p 590.
10. **Transient Thermal Processing of Silicon**, G. K. Celler and T. E. Seidel in *Silicon Integrated Circuits*, Kahng, editor, suppl. 2C to Applied Solid State Science – Advances in Materials and Device Research, (Academic Press 1985), pp. 1-73.
11. **Modification of Silicon Properties with Lasers, Electron Beams, and Incoherent Light**, G. K. Celler, *CRC Critical Reviews in Solid State and Material Sciences*, **12**, pp. 193-265 (1984).

## SCIENTIFIC ARTICLES

1. **Diffusion and Impurity Segregation in Hydrogen-Implanted Silicon Carbide**, A. Barcz, M. Kozubal, R. Jakiela, J. Ratajczak, J. Dyczewski, K. Golaszewska, T. Wojciechowski, and G. K. Celler, *J. Appl. Phys.* **115**, 223710 (2014) <http://dx.doi.org/10.1063/1.4882996>
2. **Properties of H<sup>+</sup> Implanted 4H-SiC as Related to Exfoliation of Thin Crystalline Films**, V. P. Amarasinghe, L. Wielunski, A. Barcz, L. C. Feldman, and G. K. Celler, *ECS Journal of Solid State Science and Techn.* **3** (3) P37-P42 (2014).
3. **Heteroepitaxial growth on thin sheets and bulk material: exploring differences in strain relaxation via low-energy electron microscopy**, Chanan Euaruksakul, Michelle M Kelly, Bin Yang, Donald E Savage, George K Celler, and Max G Lagally, *J. Phys. D: Appl. Phys.* **47** 025305 (2014).
4. **Lithography and doping in strained Si towards atomically precise device fabrication**, W. C. T. Lee, S. R. McKibbin, D. L. Thompson, K. Xue, G. Scappucci, N. Bishop, G. K. Celler, M. S. Carroll and M. Y. Simmons, *Nanotechnology* **25** 145302 (2014) [doi:10.1088/0957-4484/25/14/145302](https://doi.org/10.1088/0957-4484/25/14/145302)
5. **Thermal processing of strained silicon-on-insulator for atomically precise silicon device fabrication**, W.C.T. Lee, N. Bishop, D. L. Thompson, K. Xue, G. Scappucci, J. G. Cederberg, J. K. Gray, S. M. Han, G. K. Celler, M. S. Carroll, and M. Y. Simmons, *Appl. Surface. Science* **265**, pp. 833-838 (2013).
6. **Fast flexible electronics with strained silicon nanomembranes**, Han Zhou, Jung-Hun Seo, Deborah M. Paskiewicz, Ye Zhu, George K. Celler, Paul M. Voyles, Weidong Zhou, Max G. Lagally, and Zhenqiang Ma, *Scientific Reports* **3**, 1291 (2013). (DOI: 10.1038/srep01291)
7. **The influence of substrate on SOI photonic crystal thermo-optic devices**, Weiwei Song, Manjit Chahal, George K. Celler, Yogesh Jaluria, Graham T. Reed, and Wei Jiang, *Optics Express* Vol. 21, No. 4, pp.4235-4243 (2013).
8. **Pulsed Laser Assisted Exfoliation of Hydrogen Ion Implanted Single Crystalline SiC Thin Layers**, Tuğrul Özel, Thanongsak Thepsonthi, Voshadhi Amarasinghe and George K. Celler, *Proceedings of NAMRI/SME*, Vol. 41 (2013).
9. **RF model of flexible microwave switches employing single-crystal silicon nanomembranes on a plastic substrate**, Guoxuan Qin, Hao-Chih Yuan, George K. Celler, Jianguo Ma, and Zhenqiang Ma, *Microelectr. Eng.* **95**, pp. 21-25 (2012).
10. **Optimization of H<sup>+</sup> Implantation Parameters for Exfoliation of 4H-SiC Films**, V. P. Amarasinghe, L. Wielunski, A. Barcz, L. C. Feldman, and G. K. Celler, *ECS Transactions*, Vol. 50 (7), pp. 341- 348 (The Electrochemical Soc. 2012).

11. **Thermo-optic characteristics and switching power limit of slow-light photonic crystal structures on a silicon-on-insulator platform**, Manjit Chahal, George K. Celler, Yogesh Jaluria, and Wei Jiang, *Optics Express* **20**(4) 4225 (2012).
12. **Experimental characterization and modeling of the bending strain effect on flexible microwave diodes and switches on plastic substrate**, Guoxuan Qin, Laichun Yang, Jung-Hun Seo, Hao-Chih Yuan, George K. Celler, Jianguo Ma, and Zhenqiang Ma, *Appl. Phys. Lett.* **99** 243104 (2011).
13. **Influence of bending strains on radio frequency characteristics of flexible microwave switches using single-crystal silicon nanomembranes on plastic substrate**, Guoxuan Qin, Hao-Chih Yuan, George K. Celler, Jianguo Ma, and Zhenqiang Ma, *Appl. Phys. Lett.* **99**, 153106 (2011).
14. **Symmetry in Strain Engineering of Nanomembranes: Making New Strained Materials**, Deborah M. Paskiewicz, Shelley A. Scott, Donald E. Savage, George K. Celler, and Max G. Lagally, *ACS Nano* **5** (7) 5532-5542 (2011).
15. **RF model of flexible microwave single-crystalline silicon nanomembrane PIN diodes on plastic substrate**, Guoxuan Qin, Hao-ChihYuan, George K. Celler, Weidong Zhou , Jianguo Ma, Zhenqiang Ma, *Microelectronics J.* **42**, 509-514 (2011).
16. **Impact of strain on radio frequency characteristics of flexible microwave single-crystalline silicon nanomembrane p-intrinsic-n diodes on plastic substrates**, Guoxuan Qin\_ Hao-Chih Yuan, George K. Celler, Jianguo Ma, and Zhenqiang Ma, *Appl. Phys. Lett.* **97**, 233110 (2010).
17. **12-GHz Thin-Film Transistors on Transferrable Silicon Nanomembranes for High-Performance Flexible Electronics**, Lei Sun, Guoxuan Qin, Jung-Hun Seo, George K. Celler, Weidong Zhou, and Zhenqiang Ma, *Small* **6** (22), 2553-2557 (2010).
18. **Process development toward strained-Si/SiGe enhancement mode structures for quantum computing**, Nathaniel Bishop, Donald Savage, Edward S. Bielejec, Gregory Ten Eyck, Michael Lilly, Malcolm Carroll, and George K. Celler, *proceedings of ISTDM-2010*.
19. **High performance atomic-layer-deposited LaLuO<sub>3</sub> /Ge-on-insulator p-channel metal-oxide-semiconductor field-effect transistor with thermally grown GeO<sub>2</sub> as interfacial passivation layer**, J. J. Gu, Y. Q. Liu, M. Xu, G. K. Celler, R. G. Gordon, and P. D. Ye, *Appl. Phys. Lett.* **97**, 012106 (2010).
20. **Quantum Confinement, Surface Roughness, and the Conduction Band Structure of Ultrathin Silicon Membranes**, F. Chen, E. B. Ramayya, C. Euaruksakul, F. J. Himpsel, G. K. Celler, B. J. Ding, I. Knezevic, and M. G. Lagally, *ACS Nano* **4**, No. 4, pp. 2466-2474 (2010).
21. **A Review of SOI Technology and its Applications**, Bich-Yen Nguyen, George Celler, and Carlos Mazuré, *Journal Integrated Circuits and Systems* **4**, No.2, pp. 51-54 (2009).
22. **Flexible microwave PIN diodes and switches employing transferable single-crystal Si nanomembranes on plastic substrates**, Guoxuan Qin, Hao-Chih Yuan, George K Celler, Weidong Zhou, and Zhenqiang Ma, *J. Phys. D: Appl. Phys.* **42** (2009) 234006 (9pp).
23. **Substrate Engineering For 32nm And Beyond**, Bich-Yen Nguyen, Carlos Mazuré, and George Celler, *ECS Transactions* Vol. 22, No. 1, pp. 91-98 (The Electrochemical Society 2009).
24. **Nanomechanical Response of the Si Lattice to Hydrogen Implantation and Annealing for Layer Splitting**, Diefeng Gu, Helmut Baumgart, Konstantin K. Bourdelle, George K. Celler, and A. A. Elmustafa, *Japanese Journal of Applied Physics* **48**, 101202 (2009).



25. **SOI Technology Driving The 21<sup>st</sup> Century Ubiquitous Electronics**, G. K. Celler, ECS Transactions Vol. 19, issue 4, pp. 3-14, (The Electrochemical Society 2009).
26. **Bendable High-Frequency Microwave Switches Formed with Single-Crystal Silicon Nanomembranes on Plastic Substrates**, Hao-Chih Yuan, Guoxuan Qin, George K. Celler, and Zhenqiang Ma, Appl. Phys. Lett. **95**, 043109 (2009).
27. **Flexible photodetectors on plastic substrates by use of printing transferred single-crystal germanium membranes**, Hao-Chih Yuan, Jonghyun Shin, Guoxuan Qin, Lei Sun, Pallab Bhattacharya, Max G. Lagally, George K. Celler, and Zhenqiang Ma, Appl. Phys. Lett. **94**, 013102 (2009).
28. **Size and Thickness Effect on the Local Strain Relaxation in Patterned Strained Silicon-on-Insulator**, Diefeng Gu, Mingyao Zhu, George K. Celler, and Helmut Baumgart, Electrochemical and Solid-State Letters, **12** (4) H113-H116 (2009).
29. **Thermally Processed High-Mobility MOS Thin-Film Transistors on Transferable Single-Crystal Elastically Strain-Sharing Si/SiGe/Si Nanomembranes**, Hao-Chih Yuan, Michelle M. Kelly (Roberts), Donald E. Savage, Max G. Lagally, George K. Celler, and Zhenqiang Ma, IEEE Transactions on Electron Devices, Vol. 55, No. 3, (2008).
30. **Current Status And Possibilities Of Wafer-Bonding-Based Soi Technology In 45 Nm Or Below Cmos LSIs**, M. Yoshimi, D. Delprat, I. Cayrefourcq, G. Celler, C. Mazuré, B. Aspar, in Proc. 9th International Conference On Solid-State And Integrated-Circuit Technology (ICSICT), 20-23 Oct. 2008 Beijing, China (IEEE, Piscataway, NJ, USA 2008).
31. **Weakening of Hardness and Modulus of the Si Lattice by Hydrogen Implantation for Layer Transfer in Wafer Bonding Technology**, Diefeng Gu, Helmut Baumgart, Konstantin. K. Bourdelle, George Celler, and A. A. Elmustafa, ECS Transactions, **16** (8) pp. 385-391 (2008).
32. **Strain Relaxation in Patterned Strained Si-on-Insulator (sSOI) by Raman Spectroscopy**, Diefeng Gu, Helmut Baumgart, Mingyao Zhu, George Celler, ECS Transactions, **16**, (8) pp. 329-335 (2008).
33. **Effects of high-temperature anneals and <sup>60</sup>Co gamma-ray irradiation on strained silicon on insulator**, K. Park, M. Canonico, G. K. Celler, M. Seacrist, J. Chan, J. Gelpey, K. E. Holbert, S. Nakagawa, M. Tajima, and D. K. Schroder, J. Appl. Phys. **102**, 074507 (2007).
34. **Structure of elastically strain-sharing silicon (110) nanomembranes**, A. C. Opotowsky, S. A. Scott, C. S. Ritz, D. E. Savage, G. K. Celler, and M. G. Lagally, New Journal of Physics **9** (2007) 270.
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